UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,764	11/25/2003	Masashi Yonemaru	829-618	3114

23117 7590 12/22/2004

NIXON & VANDERHYE, PC
1100 N GLEBE ROAD
8TH FLOOR
ARLINGTON, VA 22201-4714

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,764	YONEMARU, MASASHI	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *21-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group II, claims 1-20 in the Paper filed 10/18/04 is acknowledged. It is noted that unpatentability of the Group II product invention would not necessarily imply unpatentability of the Group I process invention, because the product of the Group II invention could be made by a materially different process from that of the Group I invention. For example, the product of claim 1 could be made by a method for fabricating a semiconductor integrated circuit comprising the steps of *manually* synthesizing the semiconductor integrated circuit by determining a wiring pattern between a first cell comprising a plurality of transistors and a second cell comprising a PMOS transistor section and an NMOS transistor section, a wiring pattern between the plurality of transistors in the first cell, and a wiring pattern between the PMOS transistor section and the NMOS transistor section in the second cell in accordance with a predetermined scheme *using human logic and intuition, cooperation and planning, and examination of prior schemes and experimentation to test new ideas and determine their worth,* wherein the PMOS transistor section comprises a first PMOS transistor and a second PMOS transistor connected to the first PMOS transistor in series, and the NMOS transistor section comprises a first NMOS transistor and a second NMOS

transistor connected to the first NMOS transistor in series; and fabricating the *manually* synthesized semiconductor integrated circuit, a method materially different from the method of claim 21.

Applicant having elected the Group II invention without traverse, the requirement is deemed proper and is therefore made FINAL.

2. With regard to the Group II invention, this application contains claims directed to the following patentably distinct species of the claimed invention: Embodiment 2, a plurality of transistors constituting a CMOS type pass transistor logic network, shown in figures 8A-B, 9A-C and page 53 line 3 through page 56 line 13, Embodiment 3, a inverter circuit constituting a driver for various pass transistor logic networks, shown in figures 10A-B.11A-C and page 56 line 15 through page 65 line 5, Embodiment 4, an inverter circuit like Embodiment 3 but with one of the transistors connected in series having a higher threshold voltage than the other, shown in figures 13A-B and page 65 line 6 through page 66 line 17, Embodiment 5, a an inverter circuit like Embodiments 3 or 4 but with one of the transistors provided with a body potential terminal for controlling body potential, shown in figures 14A-B and page 66 line 20 through page 68 line 17, Embodiment 6, an inverter circuit with a body electrode and a gate electrode connected together, shown in figures 15A-B and page 68 line 20 through page 71 line 10, Embodiment 7, a static type data latch circuit wherein the feedback inverter circuit has no leakage current reducing function, shown in figures 16,17

and page 71 line 12 through page 74 line 20, Embodiment 8, a static type data latch circuit wherein the initial stage inverter circuit has a leakage current reducing function, shown in figures 18-19 and page 74 line 24 through page 79 line 5, Embodiment 9, a logic circuit having two or more blocks, wherein one block is operated while the other block is in stop state to reduce power consumption, shown in figure 20 and page 79 line 8 through page 85 line 13, Embodiment 10, a driver circuit in which two or more identical transistors are connected in series with their gates connected together, so that each transistor mist support only a fraction of a signal voltage, allowing higher signal voltages to be applied, shown in figures 21A-B and page 85 line 15 through page 87 line 11, and Embodiment 11, an SOI transistor having a low threshold voltage due to a steep sub-threshold characteristic, shown in figure 22 and page 87 line 14 through page 89 line 7. Note that the Group I invention claims 21-23 are drawn to Embodiments 1 and 12, which disclose methods of using an information processing apparatus within a computer to determine the arrangement of standard cells, the wiring pattern in and between cells, and the width of a wiring channel, based on a program for the control of logic circuit synthesis in a standard cell scheme, and of using an information processing apparatus within a computer to determine the arrangement of standard cells, the wiring pattern in and between cells, and the width of a wiring channel, based on a program for the control of logic circuit synthesis in a gate array cell scheme, respectively.

Embodiments 1 and 12 are not included in this election requirement. Only Embodiments 2 through 11 are included in this election requirement.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

3. Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

4. Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1913 ~~703-308-6601~~. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
11/2004

TLD 7_Dec
AU 2826